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SERIAL NO.: **09/994,446**

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ATTORNEY DOCKET NO. 10004017-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): WALKER, Richard C.

Serial No.: 09/994,446

Examiner: CORRIELUS, Jean B.

Filing Date: November 27, 2001

Group Art Unit: 2637

Title: MULTI-PHASE SAMPLING

COMMISSIONER FOR PATENTS
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Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on December 12, 2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 50-1078 the sum of $500.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 50-1078 pursuant to 37 CFR 1.25.

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Respectfully submitted,

WALKER, Richard C.

By

Daniel J. Santos
Attorney/Agent for Applicant(s)

Reg. No. 40,158

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Rev 10/04 (AplBrief)

Patent
Serial No. 09/994,446
Agilent Docket No. 10004017-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of : WALKER, Richard C.	)	
	)	
Serial No. 09/994,446	)	Group Art Unit: 2637
	)	
Filed: November 27, 2001	)	Examiner: CORRIELUS, Jean B.
	)	
For: "MULTI-PHASE SAMPLING"	)	

APPEAL BRIEF UNDER 37 C.F.R. 41.37

INTRODUCTION

This is an appeal to the Board of Patent Appeals and Interferences of the final rejection of all claims in the subject application. This Brief is in furtherance of the Notice of Appeal, filed December 12, 2005. If any further extension is required, please consider this a request therefor. The requisite fees for this Brief are enclosed. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account 50-1078.

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office at 571-273-8300 on the date indicated below.

CMcGrew — FEBRUARY 1, 2006

Carissa McGrew — **Date**

1. REAL PARTY IN INTEREST

The real party in interest is the owner of the above-referenced application, Agilent Technologies, Inc. of Palo Alto, California.

2. RELATED APPEALS AND INTERFERENCES

There are no other known appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this Appeal.

3. STATUS OF CLAIMS

Claims 1-18, 28-32 and 37-41 stand finally rejected. Claims 19-27 and 33-36 have been allowed.

The appealed claims are Claims 1-18, 28-32 and 37-41.

4. STATUS OF AMENDMENTS

No amendments have been entered subsequent to the final rejection. An After-Final Response and Amendment was filed October 6, 2005, traversing the final rejection, requesting reconsideration and amending claims 1, 10, 28, 37 and 40. These claim amendments were not entered.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention relates generally to a multi-phase sampling system and method for sampling an incoming data signal (Page 1, lines 5–8). The multi-phase sampling system has a plurality of samplers for sampling a data signal, and a multi-phase clock generator, which

generates multiple clock signals that have different phases (Page 4, lines 7 – 9). Each sampler samples the data signal in both the middle of a bit and at a transition of the bit such that the sampling system samples each bit in both the middle of the bit and at a transition of the bit (Page 6, lines 29-32; FIG. 1).

The manner in which an odd number of samplers is used to sample a data signal such that each sampler samples the data signal in both the middle of a bit and at a transition of a bit can be easily seen in FIG. 1. FIG. 1 illustrates an exemplary embodiment of the invention in which three samplers 4, 5 and 6 are used to sample an exemplary data signal 3. Sampler 4 samples the data signal at clock phase Φ0, which corresponds to the middle of bit D0, the transition T2 between bits D1 and D2, the middle of bit D3, and the transition T5 between bits D4 and D5 (Page 7, lines 6-16).

Sampler 5 samples the data signal at clock phase Φ1, which corresponds to the transition T1 between bits D0 and D1, the middle of bit D2, the transition T4 between bits D3 and D4, and the middle of bit D5. Sampler 6 samples the data signal at clock phase Φ2, which corresponds to the middle of bit D1, the transition T3 between bits D2 and D3, and the middle of bit D4 (Page 7, lines 6-16).

Due to drawing page constraints, only a portion of the exemplary data signal 3 is shown in FIG. 1. If the data signal 3 were drawn out to extend further into the right margin of the drawing page, the next sample obtained by sampler 4 would be at the middle of bit D6. The next sample obtained by sampler 5 would be at the transition T7 between bits D6 and D7. The next sample obtained by sampler 6 would be at the transition T6 between bits D5 and D6. The bit pattern of high (logic 1) and low (logic 0) bits shown in FIG. 1 is exemplary and arbitrary. For

example, although bits D1 and D2 are shown as being high, bit D1 could be high and bit D2 could be low.

Each of independent claims 1, 10, 28, 37 and 40 recite, albeit with different language, the features described above of sampling a data signal with multiple samplers that each sample the data signal when a respective clock signal of a respective phase is received by the sampler, and that each sample the data signal at a portion of the data signal corresponding to a transition of the data signal and at a portion of the data signal corresponding to data. Each of these claims also recites that the portion of the data signal corresponding to data is between consecutive transitions of the data signal.

In addition to reciting the features described above, independent claims 10, 28 and 40 also recite features of the invention relating to using the respective output signals from the samplers to determine respective phase errors, and shifting, or determining an amount by which to shift, the respective clock phases in accordance with, or based on, the respective phase errors.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed in this appeal are:

(1) Claims 1-18, 28-32 and 37-41 of the subject application stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

7. ARGUMENT

Claims 1-18, 28-32 and 37-41 Comply With the Written Description Requirement Under 35 U.S.C. § 112, First Paragraph

Claims 1-18, 28-32 and 37-41 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

(1) The Group Consisting of Independent Claims 1-18, 28-32 and 37-41

It is respectfully submitted that the Examiner has erroneously rejected these claims as failing to meet the written description requirement of 35 U.S.C. §112, first paragraph. The First paragraph of 35 U.S.C. §112 states:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The essential goal of the written description requirement is to "clearly convey the information that the applicant has invented the subject matter which is claimed." *See In re Barker*, 559 F.2d 588, 592, 194 USPQ 470, 472 (CCPA 1977). To satisfy the written description requirement, the application specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention at the time of filing. *See Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563, 19 USPQ2d 1111, 1116 (Fed. Cir. 1991). The examiner has the initial burden of presenting evidence that a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. See In re Wertheim, 541 F.2d 257, 262, 191 USPQ 96 (CCPA 1976).

The Examiner states that the specification does not provide support for the limitation recited in independent claims 1, 10, 28, 37 and 40 of "the portion of the input data signal

corresponding to data being in between two consecutive transitions of the input data signal". The Applicant respectfully disagrees for the following reasons.

The correspondence between the language contained in these claims as originally filed and the language contained in the original specification is very clear. FIG. 1 and the description provided on page 7, lines 6 – 20 describe how each sampler samples the middle of a bit and a bit transition. It is clear that the mid-bit sample corresponds to the portion of the data signal in between consecutive bit transitions. For example, sampler 4 samples the data signal in the middle of bit D0, which is in between bit transitions T0 (not shown) and T1. Likewise, the sampler 4 samples the data signal in the middle of bit D3, which is in between transitions T3 and T4. Sampler 4 also samples at the bit transitions T2 and T5.

Therefore, the Applicant respectfully submits that a person skilled in the art would understand that the claim language "the portion of the input data signal corresponding to data being in between two consecutive transitions of the input data signal" corresponds to samples of the bits, e.g., D0 – D5, in between bit transitions, e.g., T1 – T5.

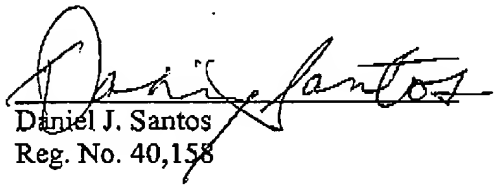
It appears that the Examiner has construed the claim term "transition" as corresponding only to a change in the data signal from high to low or from low to high. However, it is clear from the specification and FIG. 1 that the term "transition" is being used to denote a change from one bit to the next. For example, T2 is referred to as a transition on page 7, lines 11 – 12, even though the data signal remains high across the transition from bit D1 to bit D2 due to the fact that bits D1 and D2 are both logic 1s. The Applicants respectfully submit that the use of the term "transition" in the claims is identical to its use in the specification. Accordingly, the claims comply with the written description requirements, and the Applicant respectfully submits that the rejection of Claims 1-18, 28-32 and 37-41 under 35 U.S.C. §112, first paragraph, is improper.

CONCLUSION

In view of the above, it is respectfully submitted that the grounds of rejection discussed above cannot be maintained. It is therefore respectfully requested that Board reverse the decision of the Examiner rejecting Claims 1-18, 28-32 and 37-41 under 35 U.S.C. §112, first paragraph.

Respectfully submitted,

GARDNER GROFF SANTOS
& GREENWALD, P.C.



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8. Claims Appendix

1. A multi-phase sampling system having an odd number of evenly distributed clock phases, the clock phases being generated by a multi-phase clock generator, the system comprising:

a plurality of samplers, each of the samplers sampling a same input data signal when a clock signal of one of the respective phases is received by the respective sampler, each sampler sampling a portion of the input data signal corresponding to a transition of the input data signal and a portion of the input data signal corresponding to data, the portion of the input data signal corresponding to data being in between two consecutive transitions of the input data signal, each sampler outputting a respective output signal.

2. The multi-phase system of claim 1, wherein the multi-phase system comprises an odd number of said samplers.

3. The multi-phase system of claim 1, further comprising:

phase error determination circuitry, the phase error determination circuitry receiving the respective output signals and making a respective phase error determination based on each of the respective output signals.

4. The multi-phase system of claim 3, further comprising:

phase shifting circuitry, the phase shifting circuitry shifting one or more of the phases in accordance with the respective phase error determinations.

5. The multi-phase system of claim 1, wherein the multi-phase system is a receiver in communication with a multi-phase transmitter.

6. The multi-phase system of claim 1, wherein the multi-phase system is a transmitter.

7. The multi-phase system of claim 5, wherein the multi-phase system further comprises:

phase error determination circuitry, the phase error determination circuitry receiving the respective output signals and making a respective phase error determination based on each of the respective output signals, and wherein some of the phase error determinations correspond to phase errors of the multi-phase receiver and wherein some of the phase error determinations correspond to phase errors of the multi-phase transmitter.

8. The multi-phase system of claim 7, further comprising:

phase shifting circuitry, the phase shifting circuitry shifting one or more of the phases of the multi-phase receiver in accordance with the respective phase error determinations.

9. The multi-phase system of claim 7, wherein the phase error determinations that correspond to phase errors of the multi-phase transmitter are fed back to the multi-phase transmitter to enable phase shifting circuitry of the multi-phase transmitter to shift one or more of the phases of the multi-phase transmitter in accordance with the respective phase error determinations of the multi-phase transmitter.

10. A multi-phase system comprising a multi-phase clock signal generator that generates at least a first clock signal having a first phase, a second clock signal having a second phase, and a third clock signal having a third phase, the first, second and third phases being different from each other, the apparatus comprising:

a first sampling device that receives a first data signal and the first clock signal, the first sampling device comprising first sampling logic configured to sample the first data signal when the first clock signal is received by the first sampling device and to cause a first output signal to be output from the first sampling device, the first sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding

to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

a second sampling device that receives the first data signal and the second clock signal, the second sampling device comprising second sampling logic configured to sample the first data signal when the second clock signal is received by the second sampling device and to cause a second output signal to be output from the second sampling device, the second sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

a third sampling device that receives the first data signal and the third clock signal, the third sampling device comprising third sampling logic configured to sample the first data signal when the third clock signal is received by the third sampling device and to cause a third output signal to be output from the third sampling device, the third sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

phase error determination circuitry configured to determine a first phase error indication associated with the first output signal, a second phase error indication associated with the second output signal and a third phase error indication associated with the third output signal; and

phase shifting circuitry configured to shift at least one of the first, second or third phases in accordance with the respective first, second, or third phase error indications.

11. The apparatus of claim 10, wherein at least the first phase error indication is used by the phase shifting circuitry to phase-lock the multi-phase clock signal generator, and wherein the phase shifting logic shifts the second and third phases in accordance with the second and third phase error indications, respectively.

12. The apparatus of claim 10, wherein the first, second and third phase error indications are used by the phase shifting circuitry to phase-lock the multi-phase clock signal generator, and wherein the phase shifting circuitry shifts the first, second and third phases in accordance with the first, second and third phase error indications, respectively.

13. The apparatus of claim 10, wherein the phase shifting circuitry includes first, second and third charge pumps that perform modulo binning of the first, second and third phase error indications, respectively, to obtain first, second and third phase shifting values, and wherein the phase shifting circuitry shifts the first, second and third phases in accordance with the obtained first, second and third phase shift values, respectively.

14. The apparatus of claim 10, wherein the phase error determination circuitry comprises logic that is configured based on an Alexander Phase Determination Truth Table algorithm.

15. The apparatus of claim 13, wherein the phase shifting logic further includes at least first and second phase shifters configured to operate on the first and second clock signals, respectively, the first and second phase shifters receiving outputs from the first and second charge pumps, respectively, the first and second phase shifters shifting the first and second phases, respectively, in accordance with the outputs received from the first and second charge pumps, respectively.

16. The apparatus of claim 15, wherein the apparatus is incorporated into a receiver, and wherein the phase shift adjustments cause the first and second clock signals to arrive at the first and second sampling devices, respectively, at particular points in time to thereby cause the first and second sampling devices to sample the first data signal at correct points in time, the first data signal corresponding to a signal transmitted by a transmitter.

17. The apparatus of claim 15, wherein the apparatus is comprised by a receiver, and wherein the phase shift adjustments cause the first and second clock signals to arrive at the first and second sampling devices, respectively, at particular points in time to cause the first and second sampling logic to optimally sample the first data signal, the first data signal corresponding to a signal transmitted by a transmitter, the transmitter being a multi-phase system comprising a multi-phase clock generator that generates at least third, fourth, fifth, sixth and seventh clock signals having third, fourth, fifth, sixth and seventh phases, respectively, the third, fourth, fifth, sixth and seventh phases being different from each other, and wherein the phase error determination logic is also configured to determine one or more phase error indications associated with events occurring in the transmitter, and wherein the phase error indications determined to be associated with events occurring in the transmitter are transmitted by the receiver to the transmitter to enable the transmitter to adjust the third, fourth, fifth, sixth and seventh phases to eliminate phase errors in the third, fourth, fifth, sixth and seventh clock signals.

18. The apparatus of claim 15, wherein the apparatus is comprised by a transceiver, the transceiver comprising a local receiver and a local transmitter, and wherein the phase shift adjustments cause the first and second clock signals to arrive at the first and second sampling devices, respectively, at particular points to cause the first and second sampling logic to optimally sample the first data signal, and wherein the first data signal corresponds to a signal transmitted by a remote transmitter, the remote transmitter being a multi-phase system comprising a multi-phase clock generator that generates at least third, fourth, fifth, sixth and seventh clock signals having third, fourth, fifth, sixth and seventh phases, respectively, the third, fourth, fifth, sixth and seventh phases being different from each other, and wherein the phase error determination logic is also configured to determine one or more phase error indications associated with events occurring in the remote transmitter, and wherein the phase error indications determined to be associated with events occurring in the remote transmitter are transmitted by the receiver to the remote transmitter to enable the remote transmitter to adjust the third,

fourth, fifth, sixth and seventh phases to eliminate phase errors in the third, fourth, fifth, sixth and seventh clock signals, respectively.

28. A method for controlling clock phases in a multi-phase system, the multi-phase system comprising a multi-phase clock signal generator that generates at least a first clock signal having a first phase, a second clock signal having a second phase, and a third clock signal having a third phase, the first, second and third phases being different from each other, the method comprising the steps of:

sampling a first data signal with a first sampling device when the first clock signal is received by the first sampling device and outputting a first output signal from the first sampling device, the first sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

sampling the first data signal with a second sampling device when the first clock signal is received by the second sampling device and outputting a second output signal from the second sampling device, the second sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

sampling the first data signal with a third sampling device when the first clock signal is received by the third sampling device and outputting a third output signal from the third sampling device, the third sampling device sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal;

determining at least a first phase error indication associated with the first output signal, a second phase error indication associated with the second output signal and a third phase error indication associated with the third output signal;

shifting at least one of the first, second or third phases in accordance with the respective first, second or third phase error indications.

29. The method of claim 28, further comprising the step of:

phase-locking the multi-phase clock signal generator in accordance with the first phase error indication, and wherein the shifting step includes shifting at least the second and third phases in accordance with the second and third phase error indications, respectively.

30. The method of claim 28, further comprising the step of:

phase-locking the multi-phase clock signal generator in accordance with the first, second and third phase error indications, and the shifting step includes shifting the first, second and third phases in accordance with the first, second and third phase error indications, respectively.

31. The method of claim 30, wherein the step of shifting the first and second phases includes utilizing at least first and second charge pumps to perform modulo binning of the first and second phase error indications, respectively, to obtain first and second phase shifting values and shifting the first and second phases in accordance with the obtained first and second phase shift values, respectively.

32. The method of claim 28, wherein the phase errors are determined based on an Alexander Phase Determination Truth Table algorithm.

37. (Previously Presented) A method for sampling data in multi-phase sampling system having an odd number of clock phases, the clock phases being generated by a multi-phase clock generator, the method comprising the steps of:

using an odd number of samplers to sample a common input signal, each sampler sampling the input signal when a clock signal of one of said phases is received thereby, each of the sampling devices sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal, each of the sampling devices outputting a respective output signal.

38. (Original) The method of claim 37, further comprising the steps of:

receiving the respective output signals and making a respective phase error determination based on each of the respective output signals.

39. (Original) The method of claim 38, further comprising:

shifting one or more of the phases in accordance with the respective phase error determinations.

40. (Previously Presented) A computer program for reducing clock phase errors in a multi-phase system, the computer program being embodied on a computer-readable medium, the multi-phase system comprising a multi-phase clock signal generator that generates at least a first clock signal having a first phase, a second clock signal having a second phase, and a third clock signal having a third phase, the first, second and third phases being different from each other, wherein first, second and third sampling devices of the multi-phase system sample a first data signal upon receiving the first, second and third clock signals, respectively, and outputting first, second and third output signals, respectively, each of the sampling devices sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal, the computer program comprising:

a first code segment for processing the first, second and third output signals and determining first, second and third phase error indications associated with the first, second and third output signals, respectively; and

a second code segment for determining an amount by which at least one of the first, second and third phases are to be shifted based on the first, second or third phase error indications, respectively.

41. (Original) The computer program of claim 40, wherein the first code segment corresponds to an Alexander Phase Determination Truth Table algorithm.

9. Evidence Appendix

[THIS APPENDIX INTENTIONALLY LEFT BLANK][1]

[1] No "evidence" as referenced in 37 CFR 41.37(c)(1)(ix) is submitted herewith.

10. Related Proceedings Appendix

[THIS APPENDIX INTENTIONALLY LEFT BLANK][2]

[2] As stated in Section 2 of this Brief, there are no related proceedings.